REMARKS

Claims 1-5 are pending in the application.

The new title of the invention has been suggested in this Amendment.

The present invention relates to "interface device" which is connected between "CPU" and "external unit". This "interface device" has "timer portion," "mask portion" and "interrupt controlling portion". The "timer portion' asserts a mask signal, when detecting that a wait signal outputted from "external unit" is kept asserted for more than a predetermined period.

When above-mentioned mask signal is asserted, the "mask portion" masks a wait signal outputted from the "external unit". When the mask signal is asserted, the "interrupt controlling portion" issues an interrupt signal to "CPU". This architecture can prevent the system from freezing when the system bus is always occupied, even if the wait signal is kept asserted due to a trouble at the "external unit".

Claims 1-5 are rejected under 35 U.S.C.§103 as being unpatentable over Evoy in view of Miura et al. (6,477,596), newly cited.

On the other hand, Evoy (U.S. 6,062,480) discloses a system including "CARD 28", "BUS ISOLATION CIRCUIT 18" having an interface, which "CARD 28" can be attached to and removed from, and "CPU SUBSYSTEM 26" which is connected to "BUS ISOLATION CIRCUIT 18" (FIG. 1).

"BUS ISOLATION CIRCUIT 18" in Evoy does not have the same function as "timer portion" of the present invention which measures the time to transmit the wait signal from "CARD 28," and when the wait signal is kept transmitted for more than a predetermined period, the mask signal is outputted. In addition, the architecture of "BUS ISOLATION CIRCUIT 18

(BUFFER 18B of BUS ISOLATION CIRCUIT 18)" which controls "BUS 22" in Evoy is also different from that of the "mask portion" of the present invention. More specifically, "BUFFER 18B," different from the "mask portion" of the present invention as claimed, does not have the system architecture providing that the "timer portion" asserts the mask signal (as shown in Evoy (col. 3 lines 25-66, to col. 4, lines 50-64).

Miura et al (U.S. 6,477,596) discloses the architecture of the "idle mask circuit 68" which asserts IMASK signals. However, the architectures of the "idle mask circuit 68" in Miura et al. and that of "interface device" of the present invention differ from each other.

Specifically, in Miura et al. when the output-disable period of a device which is in a state of access within the current bus cycle (BC_i) is long, the basic technique is to avoid the data conflict by inserting an idle state before the next cycle (Bc_{i+1}) is adopted. When the "idle mask circuit 68" of Miura et al. detects that the same device is activating the data bus for two bus cycles continuously, the "idle mask circuit 68" asserts IMASK signals (as shown in the cited reference 2: lines 32-40, col. 5). By adopting this system architecture, in Miura et al., when the device for outputting data during the current bus cycle and the device for outputting data during the next bus cycle are the same, it is prohibited to insert an idle state after the current bus cycle. This is to avoid the data conflict from the same device.

In other words, the "idle mask circuit 68" in Miura et al. does not mask the wait signals and then issue the interrupt signals to "CPU", when the transmitting period of the wait signals continues for more than a predetermined period.

Regarding Miura et al. the basic technique of this reference relates to avoiding the data conflict on a bus. This reference does not prevent the system from freezing, when the wait signal is kept asserted due to a problem of an external device.

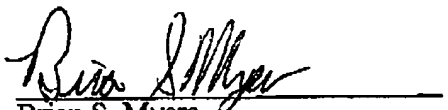
As mentioned above, even the combination of Evoy with Miura et al. would not achieve the present invention as claimed. That is to say, even if the Evoy and Miura teachings were combined, it would not be possible to obtain the effect of the present invention.

Accordingly the present invention is not obvious to a skilled artisan from the combination of Evoy with Miura et al. Therefore it is respectfully submitted that claims 1-5 pending in the application should be allowed.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



Brian S. Myers
Reg. No. 46,947

CUSTOMER NUMBER 026304
Telephone: (212) 940-8703
Fax: (212) 940-8986/8987
Docket No.: SCET 18.215 (100809-16198)
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